JMicron Technology Corporation

Product Brief

JMS581DL
USB 3.2 Gen2 to SATA 6Gb/s & PCIe Gen3 x2 Bridge Controller

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Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.00	11/14/2024	-	Initial release.	Krimmie Peng

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1 Overview

JMS581DL is a bridge controller between USB 3.2 Gen 2 10Gb/s to either SATA 6Gb/s or PCIe NVMe Gen 3x2. It combines the USB devices with both PCIe protocol and SATA protocol bridge controllers. The upstream port provides a USB 10Gb/s performance, and the downstream ports supports SATA 6Gb/s and PCIe NVMe Gen 3x2 protocol. It is able to compatible with SATA and PCIe NVMe storage devise such as HDD, SSD and CFast, CFexpress memory card. Users can easily connect their storage devices, because this controller is able to operate in USB to PCIe mode, or USB to SATA mode and switch automatically.

Moreover, JMS581DL has USB Type-C™ connectivity built in to the controller that any device using JMS581DL can have a USB Type-C™ connector without adding any additional peripheral part. It can reduce printed circuit board area for the system designs.

JMS581DL supports TRIM to the NAND flash-based storages and enable transmit and receive data by both of the USB Mass Storage Class Bulk-Only Transport (BOT) and USB Attached SCSI Protocol (UASP) to and from the host respectively. The data storage devices can achieve its summit of performance by taking advantage of these built-in unmatched features.

JMS581DL is well equipped for power management that it can meet a wide variety of power requirements from different scales of data storage systems: external storage enclosure (M.2 combo enclosure), adapter and portable storage applications.

Owing to its USB Type-C™ connectivity, JMS581DL can work with some power management controllers to a USB Power Delivery (PD) enabled data storage device. The data storage devices having SSDs of large capacity can accept the electrical power from sources of energy, such as hosts acting as a power provider of USB PD to supply sufficient electricity to the device after they negotiate with each other, without plugging in.

2 Features

2.1 General Features

- Design for Windows 7, Windows 10 and MAC 10.10.5 or later version
- Provide 8 hardware controlled PWMs
- Provide software utilities for downloading the upgraded firmware code under USB 2.0/ USB 3.2 Gen1 and USB 3.2 Gen2
- 144TFBGA (9x9mm^2) package
- Support 25MHz external crystal
- Support 3.3V I/O
- 32 GPIOs for customization

2.2 Universal Serial Bus

- Comply with USB 3.2 Gen 1 and Gen 2 Specification,
- Comply with USB Mass Storage Class, Bulk-Only Transport Specification (Revision 1.0)
- Comply with USB Attached SCSI Protocol (UASP) Specification (Revision 4)
- Integrate with USB Type-C™ multiplexer & configuration channel (CC) logic
- Support USB Super-Speed/ High-Speed/ Full-Speed Operation
- Support USB 2.0/ USB 3.2 Gen1/ Gen2 power saving mode
- Support external SPI NVRAM for Vendor VID/PID of USB 2.0/USB 3.2 Gen1/2 device controller

2.3 PCI Express

- Comply with PCI Express Base Specification Revision 3.1a
- Comply with NVM Express 1.3
- Support TRIM to the SSD

2.4 Serial ATA

- Comply with SATA Specification (Revision 3.1)
- Support TRIM to SATA
- Support Native Command Queue (NCQ)

3 Block Diagram

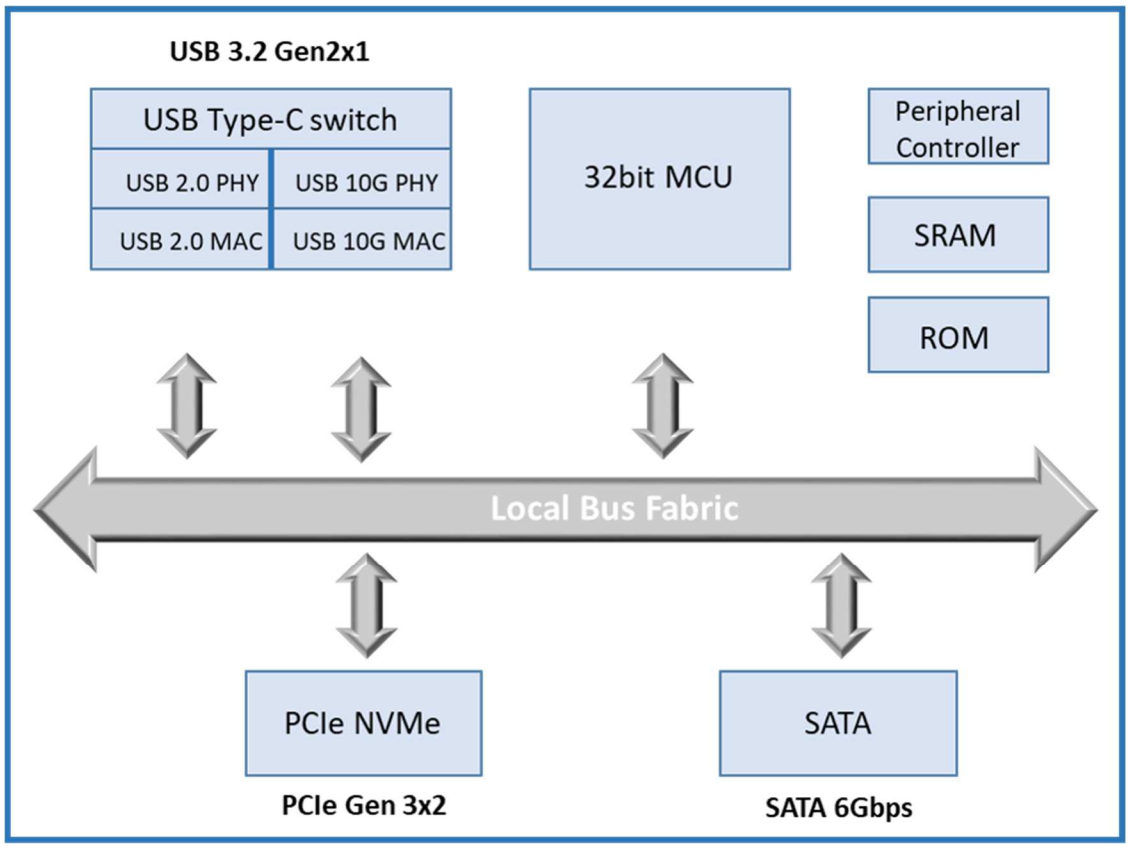


Figure 1 Block Diagram

4 Application

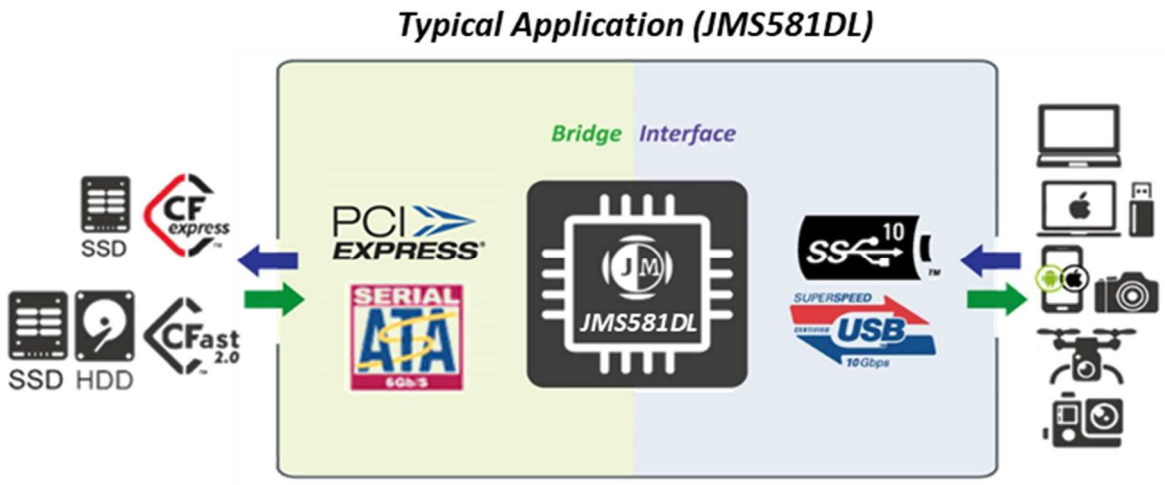
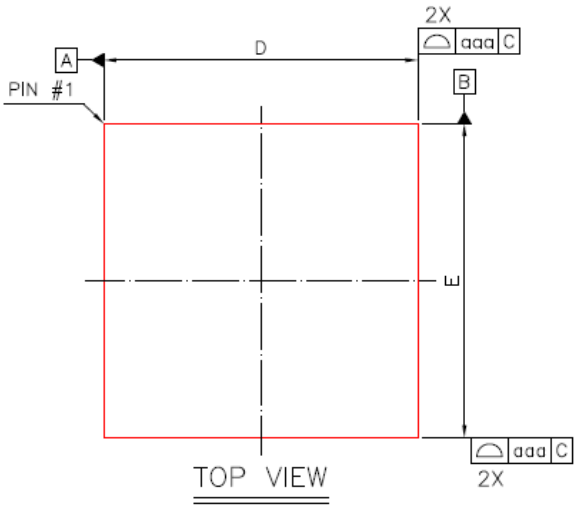


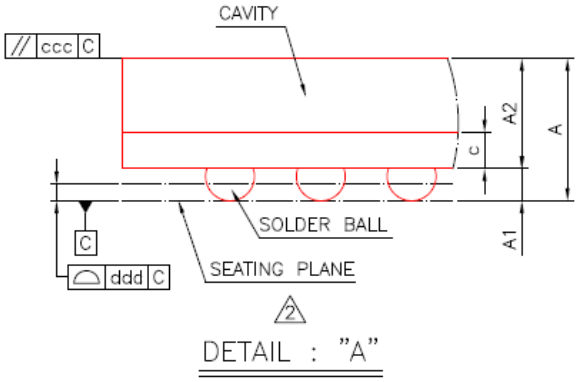
Figure 2 Application Scenarios – Dual Protocol

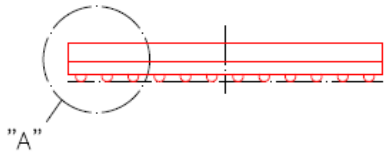
5 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.03	1.10	1.17	0.041	0.043	0.046
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
D1	---	8.25	---	---	0.325	---
E1	---	8.25	---	---	0.325	---
e	---	0.75	---	---	0.030	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		12/12				

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc,ddd(SPIL STANDARD)
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5







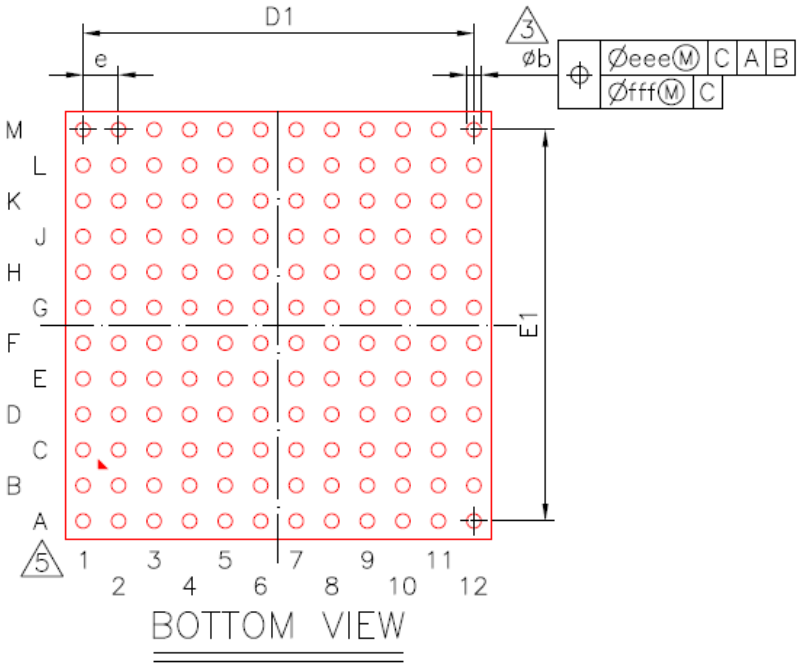


Figure 3 Package Outline Drawing of 144TFBGA 9x9mm^2

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