



Product Brief

JMS586R USB 3.2 Gen 2x2 to x2 PCIe Gen3x2 Bridge Controller with RAID0/1/ JBOD/PM

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Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
0.1	04/16/2021	--	Initial release	Joe Chang
0.2	05/13/2021	Section 1	Revised Overview section.	Katrina Mo
1.00	12/15/2021	Section 2 Section 5	Revised Features section Revised Package Dimension diagram	Katrina Mo
1.01	08/05/2024	--	Modified format. Revised Overview section.	Cora Huang

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1 Overview

JMS586R is a bridge controller between a USB host and two storage devices with a PCIe interface. The upstream port supports USB connectivity and is compliant with the USB 3.2 Gen 2x2 standard with data rates up to 20Gb/s. The downstream port supports two PCIe NVMe Gen3x2 ports. They can be connected to PCIe NVMe storage devices at data rates up to 32Gb/s, such as SSDs and memory cards. JMS586R supports the RAID0/1/JBOD function, which can improve the performance and reliability of the storages. In addition, the port multiplier function can be a cost-effective and convenient solution to expand the scalability of storage.

JMS586R integrates USB Type-C™ configuration channel (CC) logic. The device with JMS586R can use a USB Type-C™ connector without adding any additional peripheral part. JMS586R can also support external Power Delivery controller to build Power Delivery (PD) enabled data storage device. The data storage devices with large capacity SSD can accept the electrical power from sources of energy, such as hosts acting as a power provider of USB PD to supply sufficient electricity to the device after they negotiate with each other.

JMS586R supports TRIM to the SSD and can transmit and receive data by both of the USB Mass Storage Class Bulk-Only Transport (BOT) and USB Attached SCSI Protocol (UASP) to and from the host respectively. The data storage devices can achieve its summit of performance by taking advantage of these built-in unmatched features.

2 Features

2.1 General Features

- USB 3.2 Gen 2x2 to two PCIe Gen3x2 Bridge
- Design for Windows 7, Windows 10 and MAC 10.10.5 or later version
- Support firmware download through USB 2.0 / USB 3.2
- Support 25 GPIOs for customization
- Support SPI/I2C/UART/LED control with PWM
- Support 3.3V I/O
- Support 25MHz external crystal
- QFN100 10x10mm² package

2.2 Universal Serial Bus

- Comply with USB 3.2 Gen 2x2 Specification
- Support USB 3.2 Gen 2x2, up to 20Gb/s
- Integrate with USB Type-C™ multiplexer & configuration channel (CC) logic
- Support USB 2.0 / USB 3.2 Gen 1 / Gen 2 power saving mode
- Comply with USB Mass Storage Class, Bulk-Only Transport Specification (Revision 1.0)
- Comply with USB Attached SCSI Protocol (UASP) Specification (Revision 4)
- Support external SPI NVRAM for Vendor VID/PID of USB 2.0/USB 3.2 Gen 1/2 device controller
- Support SCSI command translation to NVM Express

2.3 PCI Express

- Comply with PCI Express Base Specification Revision 3.1a
- Comply with NVM Express 1.4
- Support two PCIe Gen3x2, each up to 16Gb/s
- Support TRIM to the SSD
- Support NVM Express standard command set
- Support SCSI to NVM Express pass-through command

2.4 RAID 0/ 1/ JBOD

- 2-bay PCIe Gen 3x2 NVMe SSD with RAID0/1/JBOD
- Configurable stripe size in RAID0
- Support RAID1 rebuild function
- Support PCIe SSD hot plug/unplug in RAID1

3 Block Diagram

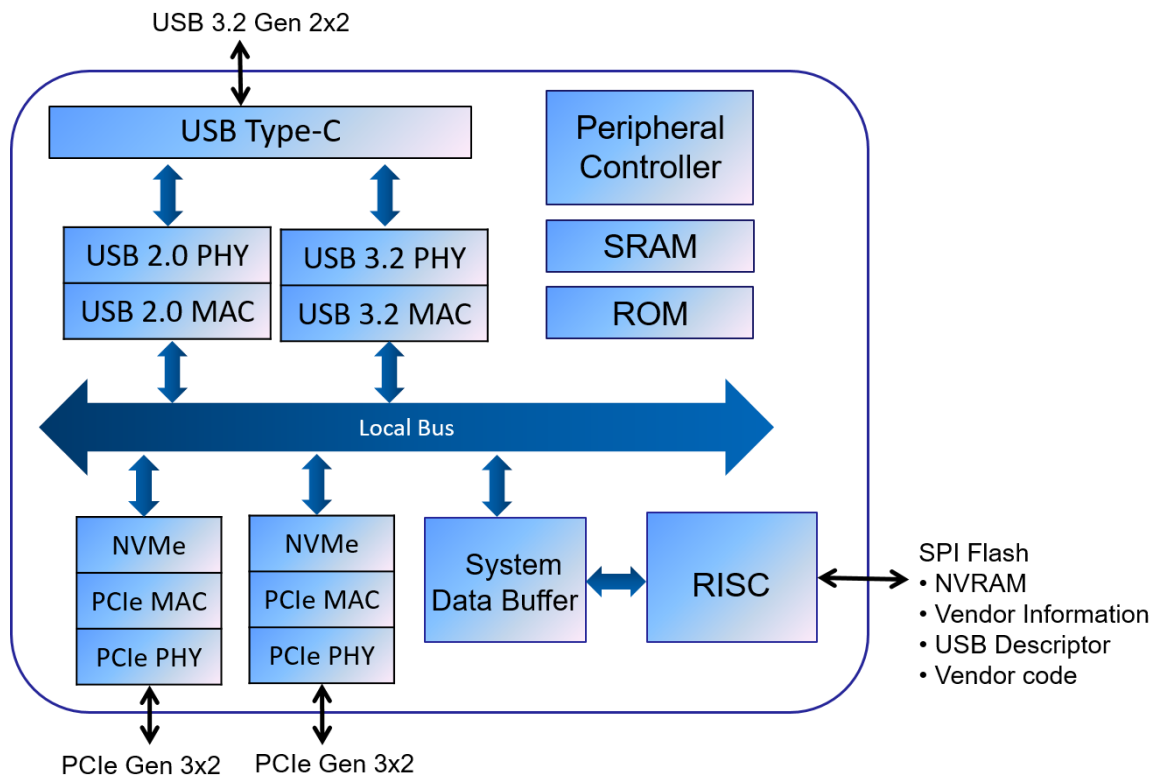


Figure 1 Block Diagram - JMS586R

4 Application

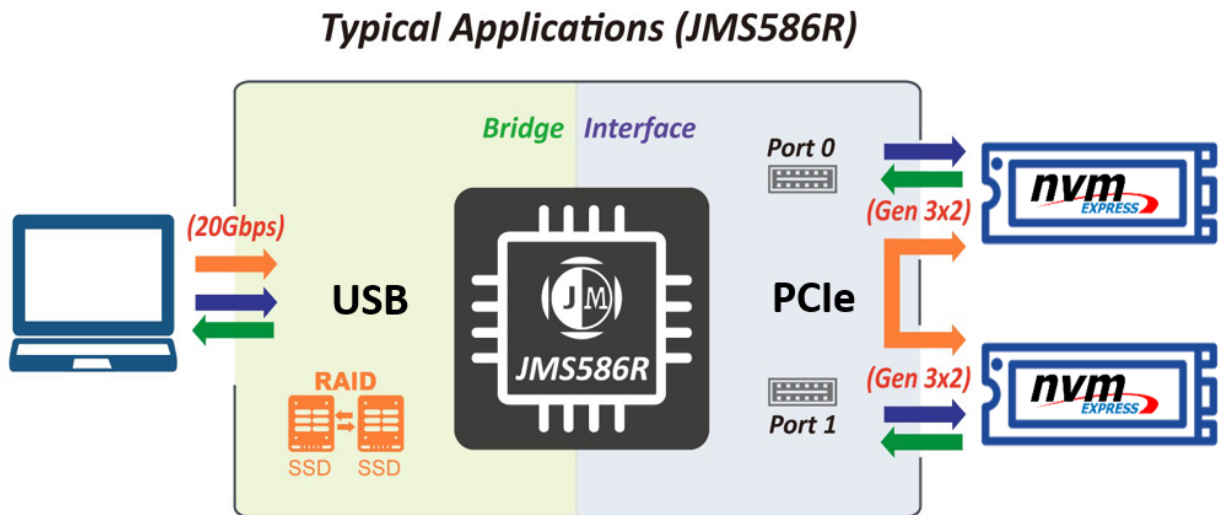
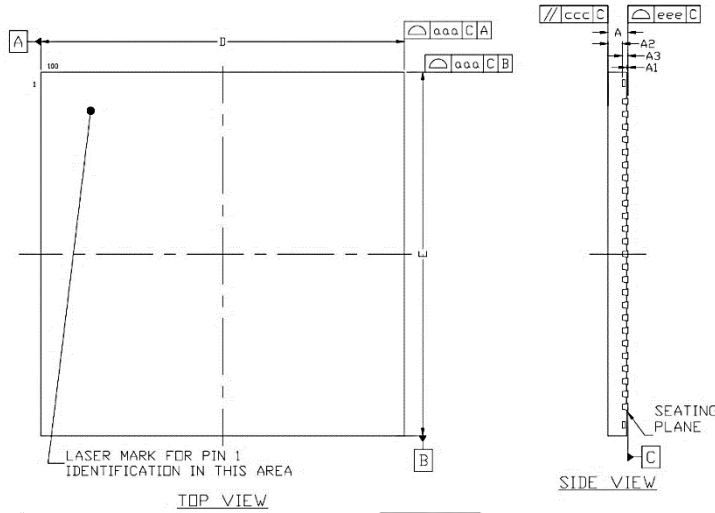


Figure 2 Application Scenarios

5 Package Dimension



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	0.900	—	—	0.035
A1	0.000	—	0.050	0.000	—	0.002
A2	—	0.650	0.700	—	0.026	0.028
A3	0.152	—	0.200	0.006	—	0.008
b	0.130	0.180	0.230	0.005	0.007	0.009
D	10	BSC	—	0.394	BSC	—
D2	7.700	—	8.800	0.303	—	0.346
E	10	BSC	—	0.394	BSC	—
E2	7.700	—	8.800	0.303	—	0.346
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.350	BSC	—	0.014	BSC	—
R	0.065	—	—	0.003	—	—
TOLERANCES OF FORM AND POSITION						
aaa	0.100	—	—	0.004	—	—
bbb	0.070	—	—	0.003	—	—
ccc	0.100	—	—	0.004	—	—
ddd	0.050	—	—	0.002	—	—
eee	0.080	—	—	0.003	—	—
fff	0.100	—	—	0.004	—	—

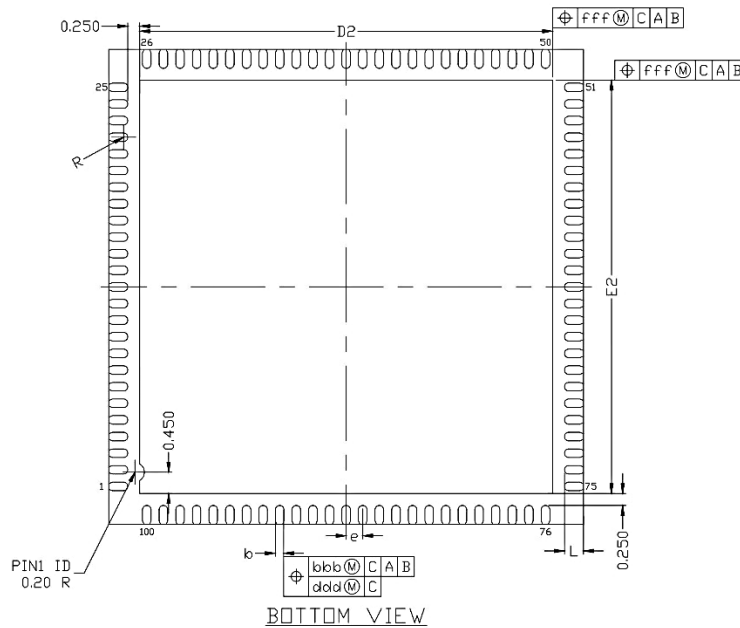


Figure 3 Package Outline Drawing

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A series of thin, light gray lines that resemble circuit traces or data paths, starting from the left and moving towards the right, with some lines curving upwards and others downwards, creating a sense of movement and connectivity.

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