



## PRODUCT BRIEF

# JMS583 USB 3.1 Gen 2 to PCIe Gen3x2 Bridge Controller

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## Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.00	5/15/2018	--	Initial release.	Joe Chang

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## 1 Overview

The JMS583 is a USB 3.1 Gen 2 to PCIe Gen3 x 2 bridge controller between USB host and PCIe storage device. The USB 3.1 Gen 2 interface offers data transfer speed up to 10Gbps, doubling the USB 3.1 Gen 1 data rate. Meanwhile, the downstream port of the JMS583 is compatible with storage device with PCIe interface, such as SSD. The PCIe port is compliant with PCIe Gen3 x 2 specifications.

The JMS583 supports TRIM command for SSD and complies with both of USB Mass Storage Class Bulk-Only Transport (BOT) and USB Attached SCSI Protocol (UASP), providing much elevated performance for data transfer between USB and PCIe devices.

USB Type-C™ connectivity is implemented in the JMS583 so that no additional component is required to enable Type-C™ connectivity when hardware system designers deploy this advanced controller. The built-in USB Type-C™ feature can save costs, PCB board space and development time for storage device developers.

The JMS583 is well equipped for power management that it can meet a wide variety of power requirements from different scales of data storage systems: those for data centers, network attached storage (NAS) systems, and portable SSDs, and even those for thumb-sized Internet-of-Thing (IoT) devices.

Finally, the JMS583 is a new product that almost reaches USB3.1 G2 line bandwidth. Using the JMS583, the security system can transfer higher quality video, such as 4K or even 8K, and quicker to their data storage devices than ever.

## 2 Features

- Integrates with USB Type-C™ multiplexer & configuration channel (CC) logic
- Supports TRIM to the SSD
- Complies with PCI Express Base Specification Revision 3.1a
- Complies with NVM Express 1.3
- Complies with USB 3.1 Gen 1 and Gen 2 Specification, USB Mass Storage Class, Bulk-Only Transport Specification (Revision 1.0)
- Complies with USB Attached SCSI Protocol (UASP) Specification (Revision 4)
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB2.0/USB 3.1 Gen 1/2 power saving mode
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB 3.1 Gen 1/2 device controller
- Thirteen GPIOs for customization
- Provides hardware controlled PWMs
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB 3.1 Gen1,2
- Design for Windows 7, Windows 10 and MAC 10.10.5 or later version
- Supports 25MHz external crystal
- Supports 3.3V I/O
- Embedded 5V to 1.0V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN64 8x8 package

### 3 Block Diagram

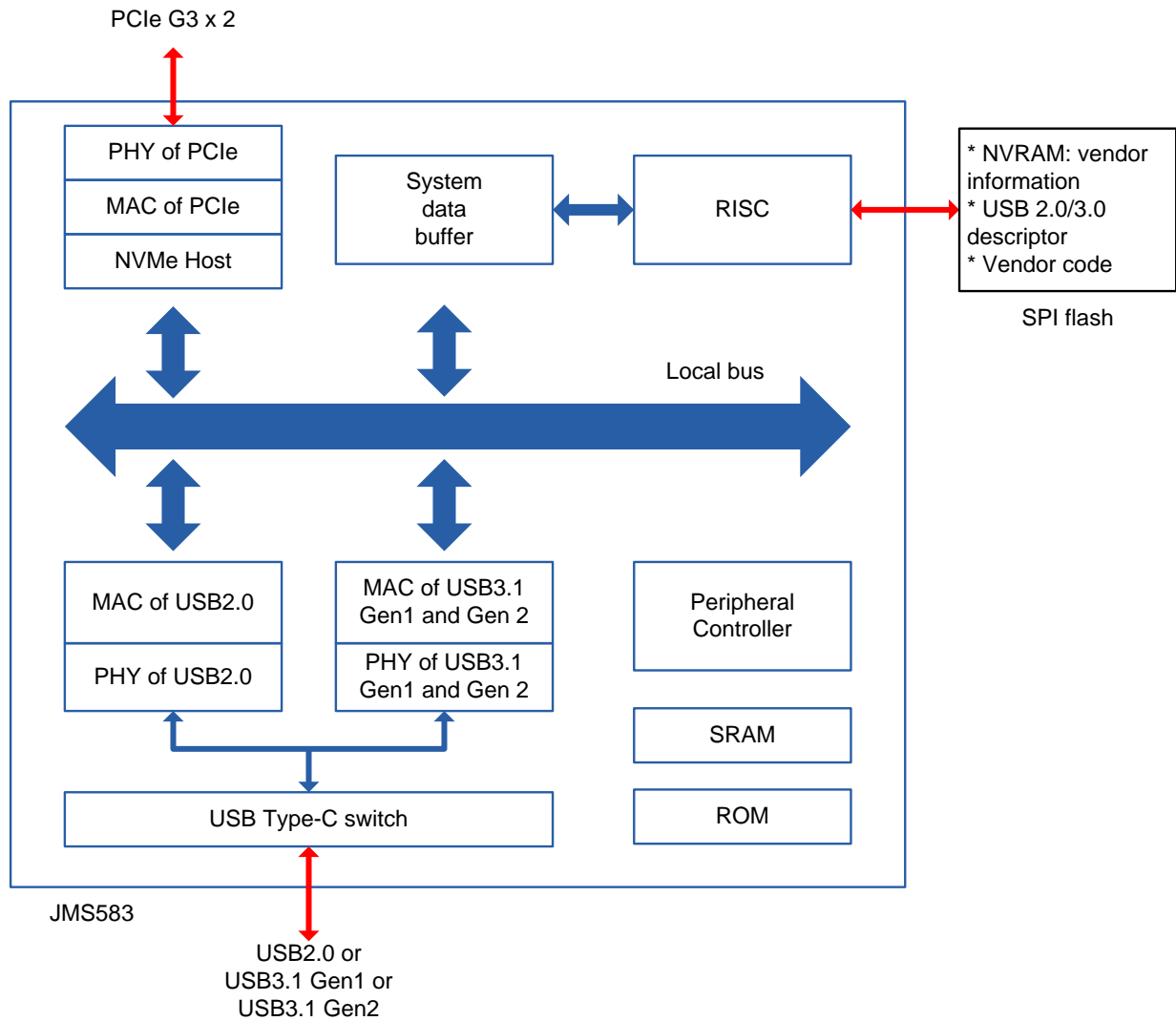


Figure 1 Block diagram

## 4 Application

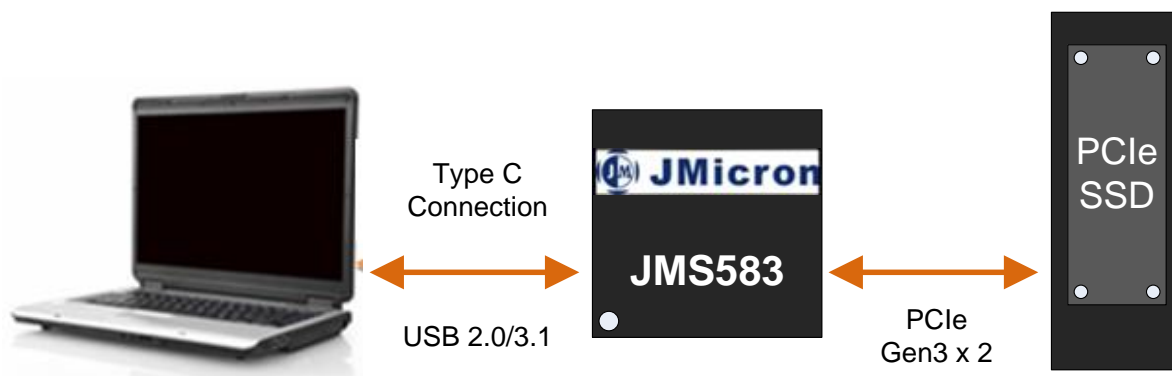
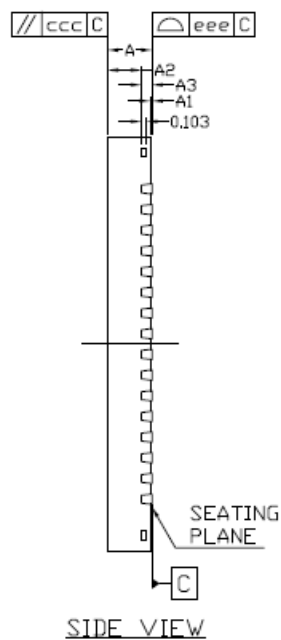


Figure 2 Illustration of an application







\* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.900	---	---	0.035
A1	0.000	---	0.050	0.000	---	0.002
A2	---	0.650	0.700	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	8.000 BSC			0.315 BSC		
D2	4.360	4.460	4.560	0.172	0.176	0.180
E	8.000 BSC			0.315 BSC		
E2	4.360	4.460	4.560	0.172	0.176	0.180
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM (0.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M, -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.

(2)

**Figure 3 Package dimension**

A series of thin, light gray lines that resemble circuit traces or data paths, starting from the left and moving towards the right, with some lines curving upwards and others downwards, creating a sense of movement and connectivity.

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