JMH330 Serial ATA Bridge Chip

Overview

The JMicron JMH330 is a single chip solution for serial and parallel ATA translation. It includes the Serial ATA PHY, Link, Transport, and parallel ATA (application layer) controller. The main applications are for serial ATA storage devices connecting to traditional IDE south bridge. For traditional IDE host, the bridge supports master only.

The Serial ATA physical, link, and transport layer are compliance to Serial ATA Generation 1, which supports a 1.5Gbps data rate. The application layer supports both the ATA register command set and PACKET command set, which could drive both the Hard Disk Drive and ATAPI Optical Storage such as CR-ROM, CD-RW, DVD-ROM, DVD-RW, etc.

The JMH330 is designed by 0.18um CMOS technology and 64-pin packages with TQFP, QFN and LQFP.

Features

■ 0.18um CMOS technology.

■ Compliance with Gen1i/Gen1m of Serial ATA II Electrical Specification 2.6.

■ 1.8V and 3.3V power system.

■ 25MHz external reference clock.

■ 64-pin TQFP, QFN and LQFP packages.

■ Support ATA/ATAPI-7 specification.

■ ATA/ATAPI PIO Mode 0, 1, 2, 3, 4.

■ ATA/ATAPI Multi-Word DMA Mode 0, 1, 2.

■ ATA/ATAPI Ultra DMA Mode 0, 1, 2, 3, 4, 5, 6, 7.

■ ATA/ATAPI PACKET command feature set.

■ ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.
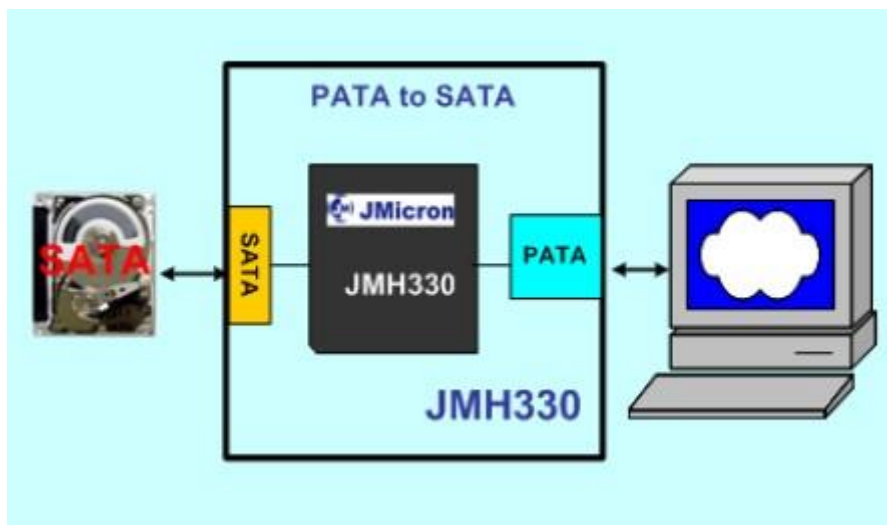
■ Serial ATA power saving modes.

Functional Block Diagram

JMH330
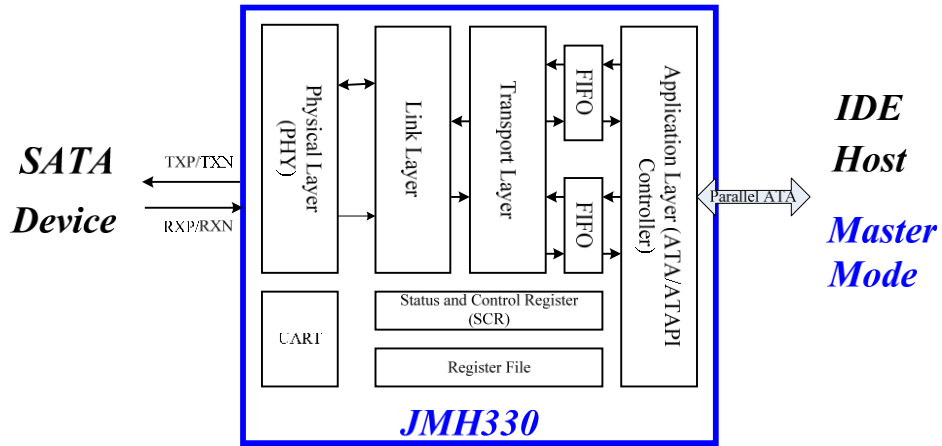
Application

Product Information

Name	Description
JMH330	Serial ATA Bridge Chip

Design Kit		Contact Information	
1	JMH330 Data Sheet	Department	Email
2	JMH330 Design Guide	Sales	sales@jmicron.com
3	Application EVB		